Qualification Process for Qorvo's Space MMIC Die

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Overview

For more than 35 years, Qorvo® has been an industry leader and supplier of highly reliable gallium arsenide (GaAs) and gallium nitride (GaN) devices for space applications, ranging from low earth orbit (LEO) missions to deep space exploration. Finding qualifiable parts or companies interested in supporting the rigorous requirements for space can be a challenge. With our heritage and experience, we help customers select space qualifiable parts and provide qualification services to our standard products and devices produced within our foundry wafer processes.

This document provides guidance on Qorvo's standard flow for screening MMIC die for space. Each subsection provides a general overview of requirements derived from MIL-PRF-38534, Table C-II, Class K. A flowchart illustrating the entire MMIC element evaluation processing flow is provided on page 4.

Qorvo strives to work closely with our customers and provide additional services when mission requirements exceed our standard flow for space qualification. When those challenges arise, we work with our customers to modify our standard flow and create a customer specific qualification. Please reach out directly to your local Qorvo representative or to the factory for quotations or any inquiries you may have regarding our space qualification process.

Subgroup 1&2

Wafer Electrical and Inspection

Wafer electrical testing and visual inspection satisfy Subgroup 1 and Subgroup 2 requirements of MIL-PRF-38534, Table C-II, Class K. Electrical testing is performed per Qorvo standard production testing on 100% of the die on wafer. All passing die and electrical rejects are identified through wafer mapping. Electrically good devices are inspected to MIL-STD-883, Method 2010, Condition A requirements. Devices meeting electrical and visual requirements are placed in gel-paks, identified as flight material, and placed in stock upon successful completion of QCI/LAT, WLAT and SEM testing.

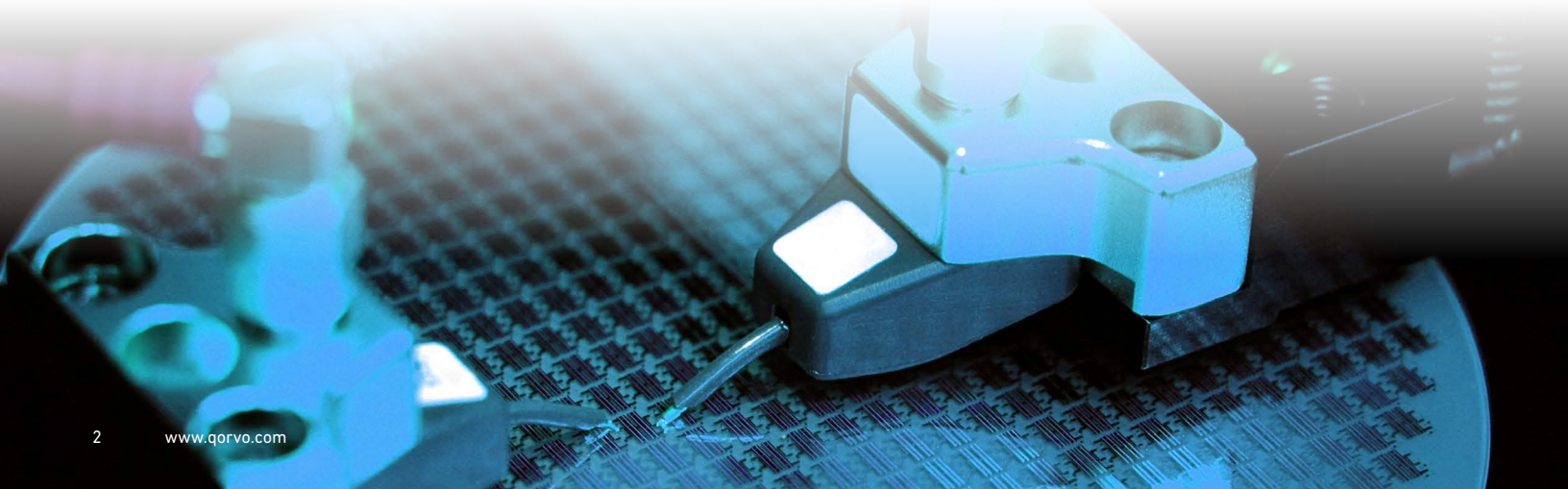
Subgroup 3&4

QCI/LAT Testing

QCI/LAT testing follows Subgroup 3 and Subgroup 4 requirements of MIL-PRF-38534, Table C-II, Class K, with the below modifications.

- Constant acceleration/mechanical shock per MIL-PRF-38534, Table C-II, Class K, Subgroup 4 is not performed
- Electrical testing is performed at room temperature only

While the identified modifications are not part of Qorvo's standard flow, they can be added to the qualification as required.



Non-Recurring Engineering (NRE)

A fixtured assembly (test vehicle) will be developed and characterized to verify stability of the device, as well as to ensure a high assembly yield for the qualification devices under test (DUTs). The junction temperature will be verified, considering the device power dissipation and the packaged assembly thermal performance. All required test procedures and associated documentation will be generated and released.

Assembly and Screening

Samples meeting Subgroup 1 and Subgroup 2 requirements are randomly selected from the wafer(s)/ wafer lot to be qualified. Each MMIC and all off-chip components are attached to the fixture eutectically with solder or with conductive epoxy, depending on the design requirements. High power dissipation assemblies are additionally inspected for voiding beneath the FET areas using radiographic imaging. DUTs are then subjected to twenty cycles of temperature cycling per MIL-STD-885, Method 1010, Condition C and visually inspected to MIL-STD-883, Method 2010, Condition B, prior to being subjected to burn-in and life testing. All samples are serialized prior to initial RF testing.

Burn-in and Life Testing

Initial testing, also known as pre burn-in testing, is done on the assembled units to set the baseline performance and to identify any assembly defects. Test parameters and conditions are defined by Qorvo and are based on the product type and performance requirements. A minimum of 10 DUTs are randomly selected, identified as QCI units and proceed onto burn-in and life testing. A minimum of three additional units are selected as calibration/archive units that will not be subjected to any additional screening and be used as control devices. The following defines the steps for burn-in and life test:

- Initial electrical test, 25°C
- Burn-in testing
    - o DC bias
    - o t = 240 hours
- Post burn-in electrical, 25°C
    - o Delta calculation
- Life test
    - o DC bias
    - o t = 1000 hours
- Final electrical test, 25°C
    - o Delta calculation

Burn-in and life testing are performed under DC bias only, at a predetermined channel temperature, based on process maximums and guidance from MIL-STD-883. Acceptance of burn-in and life test results are based on a set of delta criteria established by the product type and technology.

Subgroup 5

WLAT

Wafer lot acceptance testing (WLAT) satisfies Subgroup 5 requirements of MIL-PRF-38534, Table C-II, Class K. Samples are randomly selected from the lot to perform testing. Wire bond evaluation is performed on both the circuit side and backside of the die to MIL-STD-883, Method 2011 requirements. In addition to wire-bond evaluation, thickness measurements are taken on first metal, gate metal, glassivation, backside metallization, and overall wafer as part of our lot process monitoring.

Subgroup 6

SEM Analysis

SEM Analysis is performed as defined in Subgroup 6 requirements of MIL-PRF-38534, Table C-II, Class K.

Execution and Reporting

Qorvo's experienced internal space team will support the execution of the space die qualification (element evaluation) from quoting through delivery of the product. Results from wafer test, QCI, WLAT and SEM analysis will be summarized in reports and delivered electronically to reduce waste and support a more direct way of data transmission and retention.

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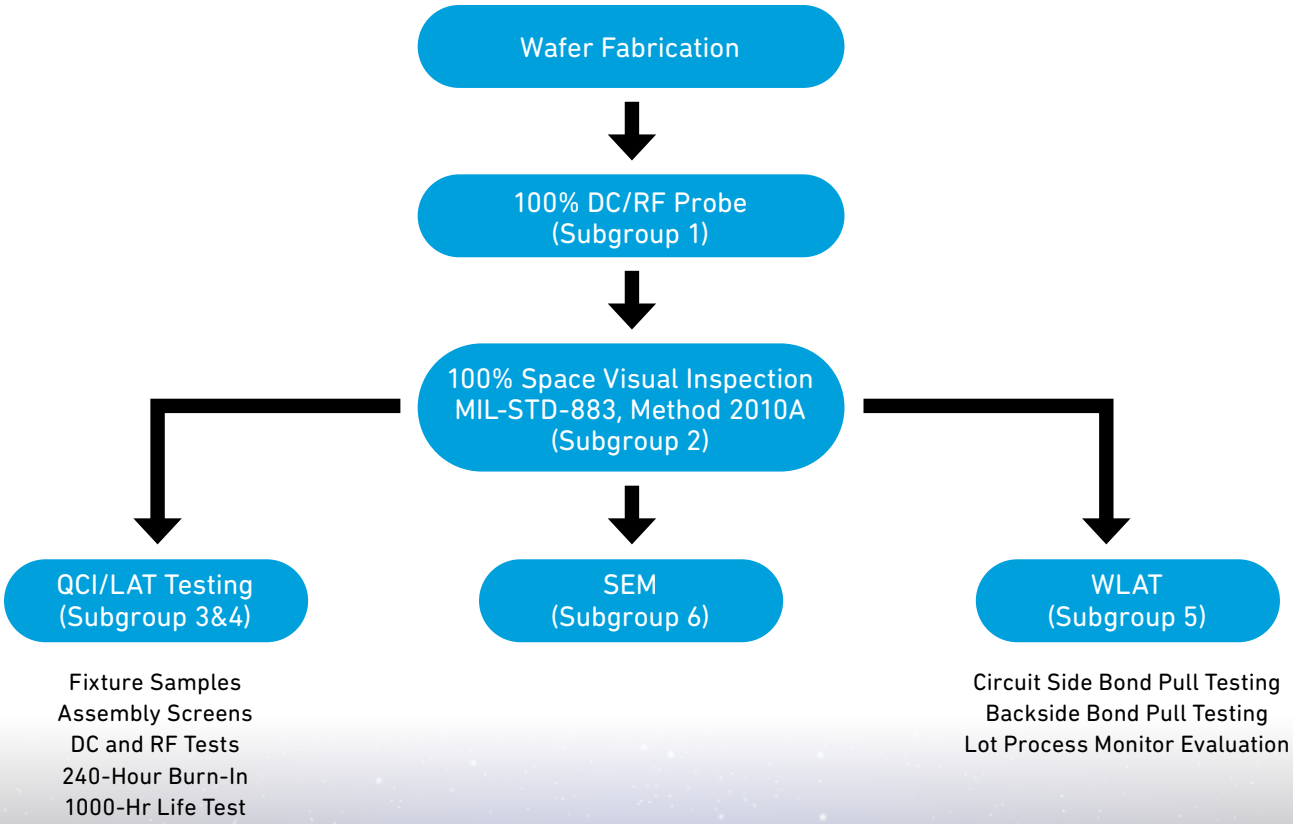
Typical Space Qualification Flowchart



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